Remarks

In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

Applicant maintains the previously-presented arguments as filed in Applicant's previous Office Action Response dated August 8, 2008, and presents the above-noted amendment without acquiescing to any of the positions presented in either the previous Final Office Action or the Advisory Action.

In the Final Office Action dated July 7, 2008, the following rejections were indicated: claims 1, 2, 5, 6, 14 and 15 were rejected under 35 U.S.C. § 103(a) over Shiga (U.S. Patent No. 6,778,443) in view of Torii (U.S. Patent No. 7,092,297); claims 3 and 4 were rejected under 35 U.S.C. § 103(a) over Shiga and Torii, and further in view of Yamazoe (U.S. Patent No. 7,009,890); claim 7 was rejected under 35 U.S.C. § 103(a) over Shiga and Torii, and further in view of Hirakawa (U.S. Patent Pub. 2001/0007541); and claims 8-13 were rejected under 35 U.S.C. § 103(a) over Shiga and Torii in view of Hirakawa and further in view of Yamazoe. Applicant respectfully traverses each of these rejections.

The § 103(a) rejection of claims 1, 2, 5, 6, 14 and 15 is improper because the proposed combination does not teach or suggest all the features recited in Applicant's claims, and because the Shiga and Torii references are not properly combinable to produce Applicant's invention. In particular, the proposed combination does not disclose a charge trapping memory device array in which substantially all of the memory devices of the array are block programmed by charging prior to being block erased by discharging. In the Final Office Action, it is admitted that the Shiga reference does not disclose programming by charging and erasing by discharging. Applicant further submits that the Shiga reference fails to teach the claimed charge trapping memory devices, and instead relates to floating gate memory devices. As Applicant has explained, Shiga's floating gate memory devices are physically and functionally different than the claimed charge trapping memory devices. Moreover, the over-erasure problem appreciated by Applicant, and that may be addressed using Applicant's invention, occurs in charge trapping memory devices, and does not occur in floating gate memory devices (*see, e.g.*, Applicant's paragraphs 0007, 0055, and 0058). The Examiner has presented no evidence

that one of skill in the art would understand how any of Shiga's teachings relating to floating gate memory devices could be applied to the programming and erasing of charge trapping memory devices, as claimed.

The Examiner has not disputed that Shiga fails to teach charge trapping memory devices, but nonetheless attempts to combine Shiga with the Torii reference, which allegedly discloses charge trapping memory devices along with programming by charging and erasing by discharging. However, Applicant finds nothing in the Torii reference to teach or suggest that one type of memory device is a suitable substitute for the other. Applicant further submits that the record contains no evidence that the memory devices of Shiga could be replaced with charge trapping memory devices, or that Applicant's claims would read on the result. Instead, the Examiner has merely relied on the unsupported and conclusory statement that Shiga would be modified to incorporate charge trapping devices that are programmed by charging and erased by discharging.

In making such a conclusion, the Examiner has ignored the teachings of the references that would lead one of skill in the art away from the proposed modifications; an approach that is contrary to settled law as stated in the M.P.E.P. § 2141.02, "A prior art reference must be considered in its entirety, *i.e.*, as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). In particular, the Examiner has ignored the teachings of Torii and Shiga that would lead one of skill in the art to understand that the proposed modifications would frustrate the stated purpose of the primary Shiga reference. It is well-settled law that if a proposed modification would render the primary reference being modified unsatisfactory for its intended purpose, then there can be no suggestion or motivation to make the modification. *See* M.P.E.P. § 2143.01 and *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

Shiga relates to pre-programming floating gate memory blocks in a manner that allows efficient and simultaneous erasing of all the blocks identified for erasure by applying the same erasing bias to all of the memory cells (*see, e.g.*, Col. 6:42-47). This avoids the long time sequences required for block-by-block erasing (*see, e.g.*, Col. 2:59-63). The Torii reference seeks to address over-erasure problems in devices such as

floating gate memory devices in which the charges injected during erasure functions accumulate in the sidewall areas between memory cells, resulting in decreased threshold voltage of the adjacent memory cells. As such, the Torii reference proposes that memory cells be erased by following a sequence in which equal and opposite bias voltages are applied to adjacent cells so that the areas between the cells do not accumulate with any particular charge. Applicant submits that the simultaneous erasing procedure taught by Shiga could not be accomplished by following the alternating procedure taught by Torii. Thus, the references are not properly combinable.

For at least the above reasons, Applicant submits that the § 103(a) rejection of claims 1, 2, 5, 6, 14 and 15 is improper.

The § 103(a) rejection of claims 3-4 is improper because the Yamazoe reference does not cure the underlying deficiencies of the proposed (and improper) combination of Shiga with Torii, and because no valid reason has been provided to make the proposed combination. The Final Office Action asserts that one of skill in the art would combine the reference cells taught by Yamazoe in the circuit taught by Shiga to control the timing of a plurality of memories based on the deterioration of the reference cell. However, the Yamazoe and Shiga references teach different types of memory devices. More specifically, Yamazoe teaches that holes or electrons are injected into a nitride film of a memory transistor. *See, e.g.,* Figures 3 and 4; Col. 1:28-35. In contrast, Shiga teaches a memory cell that has a floating gate in which electrons are trapped. *See, e.g.,* Col. 1:63 to Col. 2:3. Applicant submits that the deterioration of Yamazoe's nitride film device would not provide an indication of the deterioration of Shiga's floating gate device because these are different types of memory devices. Accordingly, there would be no motivation for one of skill in the art to combine the Yamazoe and Shiga references as proposed by the Office Action. Thus, the Office Action has not provided any evidence as to why one of skill in the art would find the asserted combination obvious as required. Therefore, the § 103(a) rejection of claims 3-4 is improper.

The § 103(a) rejection of claim 7 is improper because the Hirakawa reference does not cure the underlying deficiencies of the proposed (and improper) combination of Shiga with Torii, and because no valid reason has been provided to make the proposed combination. The Office Action states that it would be obvious to one of ordinary skill in

the art at the time the invention was made to rearrange parts of Shiga by having the reference cell in the sense amp as shown by Hirakawa. However, the Office Action fails to present any reason to support why one of skill in the art would combine Hirakawa's alleged reference cell in a sense amp with the Shiga reference. Accordingly, the Office Action has not provided any evidence as to why one of skill in the art would find the asserted combination obvious as required. Therefore, the § 103(a) rejection of claim 7 is improper.

The § 103(a) rejection of claims 8-13 is improper because the Office Action has provided no evidence of a valid reason to combine the Shiga and Torii references with the Hirakawa reference and further with the Yamazoe reference, for at least the reasons already discussed above.

Applicant further submits that the art of record fails to teach or suggest the subject matter recited in newly-added claims 16-21. In particular, Applicant finds nothing in the cited references to teach block programming and erasing prior to each data programming operation of an array of non-volatile charge trapping memory devices, as recited in claim 16. As discussed, the Shiga reference does not relate to charge trapping memory devices. Moreover, Applicant finds no teaching or disclosure that the block erase operations disclosed in the Shiga reference in any way relate to data programming operations, and instead appear to relate only to data erasing operations. Applicant also finds nothing in the cited references related to programming and erasing a reference cell each time the memory array is block programmed and erased, for example to develop matching programming and erasing histories so that a read current from the array can be compared to the reference cell and adapted accordingly, as recited in claims 17-20. Furthermore, Applicant finds nothing in the cited references to teach or suggest that the memory array is operated so that substantially none of the non-volatile charge trapping memory devices experiences two consecutive discharging cycles without experiencing an intermediate charging cycle, as recited in claim 21.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

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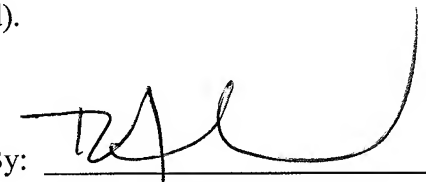
By: 

Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.330PA)